M.H

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
MP 8-13783.7 me		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/EP 99/07531	07/10/1999	09/10/1998
Applicant		
MITSUBISHI SEMICONDUCTOR EUROPE GMBH et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 2 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 3

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
/EP 99/07531

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K17/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	GB 2 319 128 A (MOTOROLA GMBH) 13 May 1998 (1998-05-13) page 1, line 24 - line 33 page 6, line 24 -page 9, line 4; figure 6	1,2, 4-14,18
Y	SENTHINATHAN R ET AL: "APPLICATION SPECIFIC CMOS OUTPUT DRIVER CIRCUIT DESIGN TECHNIQUES TO REDUCE SIMULTANEOUS SWITCHING NOISE" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 28, no. 12, 1 December 1993 (1993-12-01), pages 1383-1388, XP000435914 page 1385, right-hand column, line 7 -page 1386, left-hand column, line 11; figure 6	1,2, 4-14,18

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 January 2000	25/01/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Cantarelli, R

1

INTERNATIONAL SEARCH REPORT

[redacted]tion on patent family members

[redacted]national Application No
[redacted]T/EP 99/07531

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2319128 A	13-05-1998	NONE	

Docket No. 49,887
Express Mail: EM484715549US

PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No.

International Filing Date

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference *(if desired)-(12 characters maximum)* MP 8-13783.7 me

Box No. I TITLE OF INVENTION

MULTIPLEXER CIRCUIT AND ANALOGUE-TO-DIGITAL CONVERTER

Box No. II APPLICANT

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

MITSUBISHI SEMICONDUCTOR EUROPE GmbH
Konrad-Zuse-Straße 1

D-52477 ALSDORF
DE

☐ This person is also inventor.

Telephone No.

Facsimile No.

Teleprinter No.

State *(that is, country)* of nationality: Germany

State *(that is, country)* of residence: Germany

This person is applicant for the purposes of: ☐ all designated States ☒ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

SEIFERT, Martin
Hans-Böckler-Straße 24

DE-52477 Alsdorf
DE

This person is:

☐ applicant only

☒ applicant and inventor

☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality: Germany

State *(that is, country)* of residence: Germany

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☒ the United States of America only ☐ the States indicated in the Supplemental Box

☒ Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: ☒ agent ☐ common representative

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

PRÜFER, Lutz H.
Harthauser Straße 25d
81545 München

Telephone No. 089/640 640

Facsimile No. 089/642 22 38

Teleprinter No.

☐ **Address for correspondence:** Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Continuation of Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

If none of the following sub-boxes is used, this sheet should not be included in the request.

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

KOHN, Rüdiger
Robert-Koch-Straße 17

D-52531 Übach-Palenberg
DE

This person is:
- [ ] applicant only
- [X] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality: Germany

State *(that is, country)* of residence: Germany

This person is applicant for the purposes of:
- [ ] all designated States
- [ ] all designated States except the United States of America
- [XX] the United States of America only
- [ ] the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

GOTTSCHALK, Christoph
Paulstraße 15

D-52511 Geilenkirchen
DE

This person is:
- [ ] applicant only
- [X] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality: Germany

State *(that is, country)* of residence: Germany

This person is applicant for the purposes of:
- [ ] all designated States
- [ ] all designated States except the United States of America
- [XX] the United States of America only
- [ ] the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

This person is:
- [ ] applicant only
- [ ] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality:

State *(that is, country)* of residence:

This person is applicant for the purposes of:
- [ ] all designated States
- [ ] all designated States except the United States of America
- [ ] the United States of America only
- [ ] the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

This person is:
- [ ] applicant only
- [ ] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality:

State *(that is, country)* of residence:

This person is applicant for the purposes of:
- [ ] all designated States
- [ ] all designated States except the United States of America
- [ ] the United States of America only
- [ ] the States indicated in the Supplemental Box

- [ ] Further applicants and/or (further) inventors are indicated on another continuation sheet.

Supplemental Box *If the Supplemental Box is not used, this sheet should not be included in the request.*

1. If, in any of the Boxes, the space is insufficient to furnish all the information: in such case, write "Continuation of Box No. ..." [indicate the number of the Box] and furnish the information in the same manner as required according to the captions of the Box in which the space was insufficient, in particular:

(i) if more than two persons are involved as applicants and/or inventors and no "continuation sheet" is available: in such case, write "Continuation of Box No. III" and indicate for each additional person the same type of information as required in Box No. III. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below;

(ii) if, in Box No. II or in any of the sub-boxes of Box No. III, the indication "the States indicated in the Supplemental Box" is checked: in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the applicant(s) involved and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is applicant;

(iii) if, in Box No. II or in any of the sub-boxes of Box No. III, the inventor or the inventor/applicant is not inventor for the purposes of all designated States or for the purposes of the United States of America: in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the inventor(s) and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is inventor;

(iv) if, in addition to the agent(s) indicated in Box No. IV, there are further agents: in such case, write "Continuation of Box No. IV" and indicate for each further agent the same type of information as required in Box No. IV;

(v) if, in Box No. V, the name of any State (or OAPI) is accompanied by the indication "patent of addition," or "certificate of addition," or if, in Box No. V, the name of the United States of America is accompanied by an indication "continuation" or "continuation-in-part": in such case, write "Continuation of Box No. V" and the name of each State involved (or OAPI), and after the name of each such State (or OAPI), the number of the parent title or parent application and the date of grant of the parent title or filing of the parent application;

(vi) if, in Box No. VI, there are more than three earlier applications whose priority is claimed: in such case, write "Continuation of Box No. VI" and indicate for each additional earlier application the same type of information as required in Box No. VI;

(vii) if, in Box No. VI, the earlier application is an ARIPO application: in such case, write "Continuation of Box No. VI", specify the number of the item corresponding to that earlier application and indicate at least one country party to the Paris Convention for the Protection of Industrial Property for which that earlier application was filed.

2. If, with regard to the precautionary designation statement contained in Box No. V, the applicant wishes to exclude any State(s) from the scope of that statement: in such case, write "Designation(s) excluded from precautionary designation statement" and indicate the name or two-letter code of each State so excluded.

3. If the applicant claims, in respect of any designated Office, the benefits of provisions of the national law concerning non-prejudicial disclosures or exceptions to lack of novelty: in such case, write "Statement concerning non-prejudicial disclosures or exceptions to lack of novelty" and furnish that statement below.

Continuation of Box No. IV:

MATERNE, Jürgen
HOFER, Dorothea
Harthauser Straße 25d
81545 München

Tel.: 089/640 640
Telefax: 089/642 22 38

Box No.V DESIGNATION OF STATES

The following designations are hereby made under Rule 4.9(a) *(mark the applicable check-boxes; at least one must be marked)*:

Regional Patent

- ☐ AP **ARIPO Patent: GH Ghana, GM Gambia, KE Kenya, LS Lesotho, MW Malawi, SD Sudan, SL Sierra Leone, SZ Swaziland, UG Uganda, ZW Zimbabwe,** and any other State which is a Contracting State of the Harare Protocol and of the PCT
- ☐ EA **Eurasian Patent: AM Armenia, AZ Azerbaijan, BY Belarus, KG Kyrgyzstan, KZ Kazakhstan, MD Republic of Moldova, RU Russian Federation, TJ Tajikistan, TM Turkmenistan,** and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT
- ☒ EP **European Patent: AT Austria, BE Belgium, CH and LI Switzerland and Liechtenstein, CY Cyprus, DE Germany, DK Denmark, ES Spain, FI Finland, FR France, GB United Kingdom, GR Greece, IE Ireland, IT Italy, LU Luxembourg, MC Monaco, NL Netherlands, PT Portugal, SE Sweden,** and any other State which is a Contracting State of the European Patent Convention and of the PCT
- ☐ OA **OAPI Patent: BF Burkina Faso, BJ Benin, CF Central African Republic, CG Congo, CI Côte d'Ivoire, CM Cameroon, GA Gabon, GN Guinea, GW Guinea-Bissau, ML Mali, MR Mauritania, NE Niger, SN Senegal, TD Chad, TG Togo,** and any other State which is a member State of OAPI and a Contracting State of the PCT *(if other kind of protection or treatment desired, specify on dotted line)* .....

National Patent *(if other kind of protection or treatment desired, specify on dotted line)*:

- ☐ AE United Arab Emirates
- ☐ AL Albania .....
- ☐ AM Armenia .....
- ☐ AT Austria .....
- ☐ AU Australia .....
- ☐ AZ Azerbaijan
- ☐ BA Bosnia and Herzegovina .....
- ☐ BB Barbados
- ☐ BG Bulgaria .....
- ☐ BR Brazil .....
- ☐ BY Belarus .....
- ☐ CA Canada
- ☐ CH and LI Switzerland and Liechtenstein
- ☐ CN China .....
- ☐ CU Cuba .....
- ☐ CZ Czech Republic .....
- ☐ DE Germany .....
- ☐ DK Denmark .....
- ☐ EE Estonia .....
- ☐ ES Spain .....
- ☐ FI Finland .....
- ☐ GB United Kingdom
- ☐ GD Grenada
- ☐ GE Georgia .....
- ☐ GH Ghana .....
- ☐ GM Gambia
- ☐ HR Croatia .....
- ☐ HU Hungary .....
- ☐ ID Indonesia
- ☐ IL Israel .....
- ☐ IN India .....
- ☐ IS Iceland
- ☒ JP Japan .....
- ☐ KE Kenya .....
- ☐ KG Kyrgyzstan .....
- ☐ KP Democratic People's Republic of Korea .....
- ☐ KR Republic of Korea .....
- ☐ KZ Kazakhstan .....
- ☐ LC Saint Lucia
- ☐ LK Sri Lanka
- ☐ LR Liberia
- ☐ LS Lesotho .....
- ☐ LT Lithuania
- ☐ LU Luxembourg
- ☐ LV Latvia
- ☐ MD Republic of Moldova .....
- ☐ MG Madagascar .....
- ☐ MK The former Yugoslav Republic of Macedonia .....
- ☐ MN Mongolia
- ☐ MW Malawi .....
- ☐ MX Mexico .....
- ☐ NO Norway
- ☐ NZ New Zealand .....
- ☐ PL Poland .....
- ☐ PT Portugal .....
- ☐ RO Romania
- ☐ RU Russian Federation .....
- ☐ SD Sudan
- ☐ SE Sweden
- ☐ SG Singapore
- ☐ SI Slovenia .....
- ☐ SK Slovakia .....
- ☐ SL Sierra Leone .....
- ☐ TJ Tajikistan .....
- ☐ TM Turkmenistan .....
- ☐ TR Turkey .....
- ☐ TT Trinidad and Tobago .....
- ☐ UA Ukraine .....
- ☐ UG Uganda .....
- ☒ US United States of America .....
- ☐ UZ Uzbekistan .....
- ☐ VN Viet Nam .....
- ☐ YU Yugoslavia .....
- ☐ ZA South Africa .....
- ☐ ZW Zimbabwe .....

Check-boxes reserved for designating States which have become party to the PCT after issuance of this sheet:

- ☐ .....
- ☐ .....

Precautionary Designation Statement: In addition to the designations made above, the applicant also makes under Rule 4.9(b) all other designations which would be permitted under the PCT except any designation(s) indicated in the Supplemental Box as being excluded from the scope of this statement. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. *(Confirmation of a designation consists of the filing of a notice specifying that designation and the payment of the designation and confirmation fees. Confirmation must reach the receiving Office within the 15-month time limit.)*

Box No. VI PRIORITY CLAIM ☐ Further priority claims are indicated in the Supplemental Box.

Filing date of earlier application (day/month/year)	Number of earlier application	Where earlier application is: national application: country	regional application:* regional Office	international application: receiving Office
item (1) 09/10/1998	98 119 148.9		EP Application Regional Office = EPO	
item (2)				
item (3)				

☐ The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) *(only if the earlier application was filed with the Office which for the purposes of the present international application is the receiving Office)* identified above as item(s): _____

* *Where the earlier application is an ARIPO application, it is mandatory to indicate in the Supplemental Box at least one country party to the Paris Convention for the Protection of Industrial Property for which that earlier application was filed (Rule 4.10(b)(ii)). See Supplemental Box.*

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(if two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used):* ISA /

Request to use results of earlier search; reference to that search *(if an earlier search has been carried out by or requested from the International Searching Authority):*

Date *(day/month/year)* Number Country *(or regional Office)*

Box No. VIII CHECK LIST; LANGUAGE OF FILING

This international application contains the following **number of sheets**:

request	:	5
description (excluding sequence listing part)	:	11
claims	:	4
abstract	:	1
drawings	:	5
sequence listing part of description	:	
Total number of sheets	:	26

This international application is **accompanied by** the item(s) marked below:

1. ☒ fee calculation sheet
2. ☐ separate signed power of attorney will follow
3. ☐ copy of general power of attorney; reference number, if any:
4. ☐ statement explaining lack of signature
5. ☐ priority document(s) identified in Box No. VI as item(s): (1) will follow
6. ☐ translation of international application into (language):
7. ☐ separate indications concerning deposited microorganism or other biological material
8. ☐ nucleotide and/or amino acid sequence listing in computer readable form
9. ☒ other *(specify)*: Cheque No. 4700001406595

Figure of the drawings which should accompany the abstract: 2

Language of filing of the international application: English

Box No. IX SIGNATURE OF APPLICANT OR AGENT

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request).

Dorothea Hafer

Professional Representative

For receiving Office use only

1. Date of actual receipt of the purported international application:
2. Drawings: ☐ received: ☐ not received:
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:
4. Date of timely receipt of the required corrections under PCT Article 11(2):
5. International Searching Authority (if two or more are competent): ISA /
6. ☐ Transmittal of search copy delayed until search fee is paid.

For International Bureau use only

Date of receipt of the record copy by the International Bureau:

PATENT COOPERATION TREATY

Express Mail: EM484715549US
Docket No. 49,887

From the INTERNATIONAL BUREAU

PCT

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

To:
PRÜFER, Lutz, H.
Harthauser Strasse 25d
D-81545 München
ALLEMAGNE

Date of mailing (day/month/year)	
20 April 2000 (20.04.00)	
Applicant's or agent's file reference	**IMPORTANT NOTICE**
MP 8-13783.7 me	

International application No.	International filing date (day/month/year)	Priority date (day/month/year)
PCT/EP99/07531	07 October 1999 (07.10.99)	09 October 1998 (09.10.98)

Applicant MITSUBISHI SEMICONDUCTOR EUROPE GMBH et al

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:

   JP,US

   In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:

   EP

   The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on

   20 April 2000 (20.04.00) under No. WO 00/22730

REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, **a demand for international preliminary examination** must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the **national phase**, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer
J. Zahra

Telephone No. (41-22) 338.83.38

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 :
H03K 17/16

A1

(11) International Publication Number: WO 00/22730

(43) International Publication Date: 20 April 2000 (20.04.00)

(21) International Application Number: PCT/EP99/07531

(22) International Filing Date: 7 October 1999 (07.10.99)

(30) Priority Data:
98119148.9 9 October 1998 (09.10.98) EP

(71) Applicant *(for all designated States except US)*: MITSUBISHI SEMICONDUCTOR EUROPE GMBH [DE/DE]; Konrad–Zuse–Strasse 1, D–52477 Alsdorf (DE).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: SEIFERT, Martin [DE/DE]; Hans–Böckler–Strasse 24, D–52477 Alsdorf (DE). KOHN, Rüdiger [DE/DE]; Robert–Koch–Strasse 17, D–52531 Übach–Palenberg (DE). GOTTSCHALK, Christoph [DE/DE]; Paulstrasse 15, D–52511 Geilenkirchen (DE).

(74) Agents: PRÜFER, Lutz, H. et al.; Harthauser Strasse 25d, D–81545 München (DE).

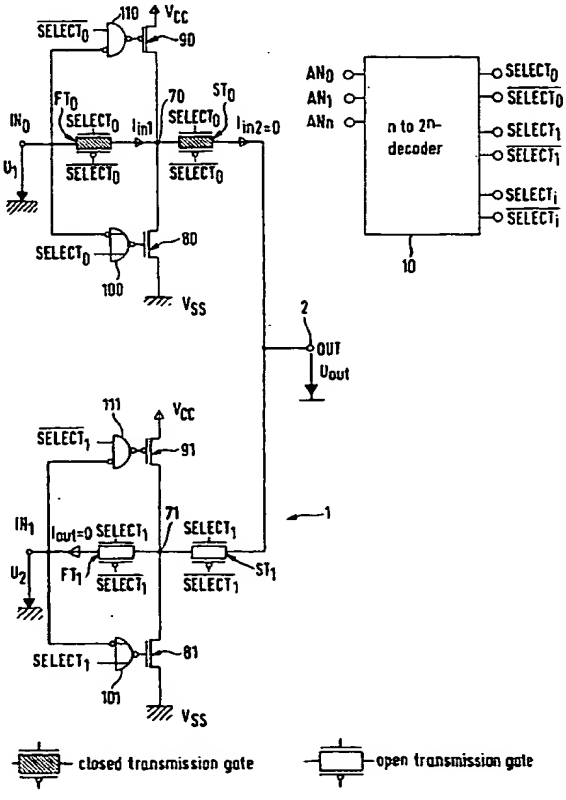
(81) Designated States: JP, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: MULTIPLEXER CIRCUIT AND ANALOGUE–TO–DIGITAL CONVERTER

(57) Abstract

A multiplexer circuit (100) comprises at least two input channels (IN_0, IN_1) and an output channel (2), each input channel (IN_0, IN_1) comprising a first transmission gate (FT_0, FT_1) which can be switched by a select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) for connecting the input channel (IN_0, IN_1) to the output channel (2), and wherein at least one of the input channels (IN_0, IN_1) comprises a bypass circuit for preventing a current flowing through the first transmission gate (FT_0, FT_1) from reaching the other input channel, and a second transmission gate (ST_0, ST_1).



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MULTIPLEXER CIRCUIT AND ANALOGUE-TO-DIGITAL CONVERTER

The invention relates to a multiplexer circuit according to the preamble of claim 1 and to an analogue-to-digital converter (ADC)comprising such a multiplexer circuit.

In monolithic IC's transmission gates can be used for multiplexer circuits. They are suitable to select one of several analogue input channels to connect the selected channel, for example, to an ADC circuit on chip. Multiplexer circuits built with transmission gates implemented in monolithic IC's with MOS (metal oxide semiconductor) type circuits are known from CMOS Digital Integrated Circuits, Analysis and Design, S.M. Kang, Y. Leblebici, McGRAW-HILL INTERNATIONAL EDITIONS, ISBN 0-07-038046-5, page 274 and from Principles of CMOS VLSI Design, A System Perspective, second edition ADDISON WESLEY, N.H.E., Weste, K. Eshraghian, ISBN 0-201-53376-6, pages 17, 304.

An example of a conventional multiplexer circuit 1 comprising transmission gates is shown in Fig. 5. The multiplexer circuit 1 comprises at least two input channels IN_0, IN_1 which are connected with a common output channel 2. Of course, a plurality of input channels IN_0, IN_1, IN_2,... IN_i may be provided in the multiplexer circuit. For selecting one of said analogue input channels IN_0, IN_1 the multiplexer circuit comprises transmission gates FT_0, FT_1 between the input channel IN_0, IN_1 and the output channel 2, respectively. The

multiplexer can select one of the two input channels IN_0, IN_1 by select signals $SELECT_0$, $\overline{SELECT_0}$, $SELECT_1$, $\overline{SELECT_1}$ generated by a decoder circuit 10. The decoder circuit generates a select signal $SELECT_0$, $SELECT_1$ and an inverted select signal $\overline{SELECT_0}$, $\overline{SELECT_1}$ for each input channel IN_0, IN_1, respectively, which are applied to the corresponding transmission gates FT_0, FT_1. The decoder circuit is a n to 2^n decoder ($i = 2^n$), which ensures that only one of the select signals $SELECT_0$ to $SELECT_i$ becomes true while the others are false, i.e. only one channel is open while the others are closed. In the example according to Fig. 4 the channel IN_1 is selected i. e. the transmission gate FT_1 is open, whereas the channel IN_0 is not selected and the transmission gate FT_0 is closed. Analog voltages U_1, U_2 are applied to the input channels IN_0, IN_1, respectively. The voltage at the output channel 2 is indicated as U_{out}. The transmission gates FT_0, FT_1 are known CMOS transmission gates comprising p channel and n channel transistors having threshold voltages V_{THp} and V_{THn}, respectively. The multiplexer circuit is operated with a power supply voltage V_{CC} and V_{SS} is the ground potential 0V.

The operation of the multiplexer circuit is as follows. In a normal operation condition the following input voltage conditions are applied:

$$U_1 = [V_{SS}; V_{CC}]$$
$$U_2 = [V_{SS}; V_{CC}].$$

That means the level of the input voltages U_1, U_2 is between the power supply voltage level V_{CC} and V_{SS}.

Under these conditions the transmission gates FT_0 and FT_1 operate as ideal switches. Since the transmission gate FT_0 is closed, the voltage U_{out} is equal to U_2:

$$U_{out} = U_2.$$

No current will flow in the multiplexer circuit, i.e. the current in the channels IN_0 and IN_1 is 0, respectively:

$$I_{in1} = 0$$
$$I_{out} = 0.$$

In case of an over or an under voltage applied to an input channel which is not selected i. e. which is not active a current will flow through the active channel. This is the under/over voltage operation condition. The following input voltage conditions are considered as under and over voltage conditions:

Under voltage:

$$-V_{THn} + V_{SS} \leq U_1 \leq V_{SS}.$$

Over voltage:

$$V_{CC} \leq U_1 \leq V_{CC} + |V_{THp}|,$$

The voltage U_2 is:

$$U_2 = [V_{SS}; V_{CC}].$$

Under these conditions the transmission gate FT_0 in channel IN_0 does not work as an ideal switch any more. Due to "weak inversion" and the pn-diode structures of the CMOS transistors a current flows between IN_0 and IN_1.

$$\begin{vmatrix} I_{in} \\ I_{out} \end{vmatrix} \geq 0$$

I_{out} creates a voltage drop at the resistance of the transmission gate FT_1 in channel IN_1 and the output resistance of the source of U_2. Therefore, U_{out} is not equal to the input voltage U_2 any more. Depending on the desired accuracy of the analogue signal this will be a problem.

In particular for multiplexer circuits used in ADC's a noise at the injection source leads to worse accuracy, which makes the conversion results unusable (e.g. in case of an 8-bit ADC the absolute accuracy becomes 10-11 LSB instead of +/-2 LSB). External over/undervoltage protection circuits are required in order to be able to use such ADC's.

It is an object of the invention to provide a multiplexer circuit and an analogue-to-digital converter having an improved accuracy with respect to the output of an analogue input signal.

The object is solved by a multiplexer circuit according to claim 1 and by an analogue-to-digital converter according to claim 12. Further developments of the invention are described in the dependent claims.

Embodiments of the invention will be explained with reference to the accompanying drawings.

Fig. 1 shows a multiplexer circuit according to a first embodiment of the invention.

Fig. 2 shows a multiplexer circuit according to a second embodiment of the invention.

Fig. 3 shows a multiplexer circuit according to the second embodiment of the invention more in detail.

Fig. 4 shows a multiplexer circuit according to a further embodiment of the multiplexer circuit of Fig. 2.

Fig. 5 shows an example of a conventional multiplexer circuit.

A first embodiment of the multiplexer circuit according to the invention is shown in Fig. 1. Parts which are the same as in the conventional multiplexer circuit according to Fig. 4 are

designated with the same reference signs and the description thereof will not be repeated.

The multiplexer circuit according to this embodiment comprises a first transmission gate FT_0, FT_1, for each channel respectively, and a second transmission gate ST_0, ST_1 for each channel. The output of the first transmission gate FT_0, FT_1 in each channel is connected with the input of the second transmission gates ST_0, ST_1, respectively. The output of the second transmission gate ST_0 and ST_1 is connected with the output channel 2. The second transmission gate ST_0, ST_1 are controlled by the same select signals $SELECT_0$, $\overline{SELECT_0}$ and $SELECT_1$, $\overline{SELECT_1}$ as the first transmission gates FT_0, FT_1.

A bypass circuit in form of an NMOS transistor 20, 21 is provided for each analogue input channel IN_0, IN_1. Each NMOS transistor 20, 21 is connected with its drain to a node 30 31. Each node 30, 31 is connected with the output of the first transmission gate FT_0, FT_1 and the input of the second transmission gate ST_0, ST_1, respectively. The source of each NMOS transistor 20, 21 is connected with the ground potential level V_{SS}. The gate of each NMOS transistor receives the inverted select signal $\overline{SELECT_0}$, $\overline{SELECT_1}$, respectively, which is generated by the channel decoder 10. In this embodiment the NMOS transistors are controlled by the same select signal as the PMOS transistor of the transmission gates.

In the example according to Fig. 1 the channel IN_1 is selected and the first transmission gate FT_1 and the second transmission gate ST_1 are both open. Since the NMOS transistor 21 receives the inverted select signal $\overline{SELECT_1}$ on its gate, the NMOS transistor 21 is switched off for the selected channel IN_1. The channel IN_0 is not selected and therefore, the first transmission gate FT_0 and the second transmission gate ST_0 are both closed. Since the NMOS transistor 20 receives the inver-

ted select signal $\overline{SELECT_0}$ on its gate, the NMOS transistor 20 is switched on for the not selected channel IN_0.

In operation the select signals are applied to the transmission gates such that the input channel IN_1 is selected by opening the first transmission gate FT_1 and the second transmission gate ST_1 by the select signal $SELECT_1$ ($SELECT_1 = 1$). The other input channel IN_0 is not selected by closing the first transmission gate FT_0 and the second transmission gate ST_0 by applying the select signal $SELECT_0$ ($SELECT_0 = 0$).

In case the voltage U_1 applied to the first input channel IN_0 has an over voltage i.e.

$$V_{CC} \leq U_1 \leq V_{CC} + |V_{THp}|,$$

a current I_{in1} flows through the first transmission gate FT_0 to node 30. Since the NMOS transistor 20 is switched on by the select signal $\overline{SELECT_0}$, the current I_{in1} is bypassed through the NMOS transistor 20 to ground. The potential at node 30 is (due to being pulled down by NMOS transistor 20) in the range of $[0, V_{CC}]$. Therefore, the transmission gate ST_0 operates as an ideal switch, i.e. closes perfectly. Therefore, the selected input channel IN_1 is not influenced by the over voltage on the first input channel IN_0. The output voltage U_{out} is equal to U_2.

Without changing the circuit in Fig. 1 the NMOS transistor 20 pulls an undervoltage $-V_{TH,N} < U_1 < 0$ at the input to a potential in the range of $[-V_{TH,N}, 0]$ at node 30. This is enough to switch the transmission gate ST_1 off and to avoid influence to the analogue input. Hence, the NMOS transistor is a measure against under voltage. However, the bypass behaviour of the NMOS transistor for over voltage condition is better than for under voltage condition.

Fig. 2 shows an embodiment of a multiplexer circuit in order to bypass the current for over or under voltage conditions. In

the embodiment according to Fig. 2 parts which are equal to parts of the embodiment according to Fig. 1 are described with the same reference signs. The multiplexer circuit according to Fig. 2 comprises a pull-down bypass circuit 50, 51 in each channel IN_0, IN_1 and in addition a pull-up bypass circuit 60, 61. The pull-down bypass circuit 50, 51 is connected between a node 70, 71 and V_{SS} level and the pull-up bypass circuit 60, 61 is connected between the node 70, 71 and V_{CC} level, respectively.

The multiplexer circuit according to Fig. 2 also comprises two operation conditions: In the normal operation condition the following input voltage conditions are applied:

$$U_1 = [V_{SS}; V_{CC}]$$
$$U_2 = [V_{SS}; V_{CC}].$$

Under these conditions the transmission gates operate as ideal switches. The voltage U_{out} is equal to U_2. No current will flow:

$$I_{in1} = 0$$
$$I_{out} = 0.$$

In an under/over voltage operation condition the following input voltage conditions are considered as under and over voltage conditions:

Under voltage:

$$-V_{THn} + V_{SS} \leq U_1 \leq V_{SS}$$

Over voltage:

$$V_{CC} \leq U_1 \leq V_{CC} + |V_{THp}|$$

(V_{THn}, V_{THp} are threshold voltages of p- and n channel transistors)

The voltage U_2 is:

$$U_2 = [V_{SS};\ V_{CC}].$$

Under these conditions the first transmission gate FT_0 in channel IN_0 does not work as an ideal switch. The current I_{in1} is bypassed to V_{SS} level or V_{CC} level by using the bypass circuit 50 or 60. The second transmission gate ST_0 is implemented in order not to change the U_{out} voltage. In case of an over/under voltage condition the bypass circuit 50 reduces the input voltage for the second transmission gate ST_0, so that no over voltage condition occurs at the second transmission gate ST_0 and the bypass circuit 60 increases the input voltage for the second transmission gate, so that no under voltage condition occurs at the second transmission gate ST_0. Therefore, the second transmission gate will work again as an ideal switch. As a result no current flows between IN_0 and IN_1 and the voltage U_{out} is equal to the input voltage U_2, i.e.

$$\begin{aligned} |I_{in1}| &\geq 0 \\ |I_{in2}| &= 0 \\ |I_{out}| &= 0 \\ U_{out} &= U_2. \end{aligned}$$

An additional circuit senses either the voltage in front of FT_0 or between FT_0 and ST_0 and switches on either the bypass circuit to V_{CC} in case of under voltage or the bypass circuit to V_{SS} in case of over voltage. This is necessary to avoid a shortcut between V_{CC} and V_{SS} via the two bypass circuits. The combination of the bypass circuit and the sense circuit forms a bypass and sense circuit.

In a further development the bypass and sense circuit contains elements to control the potential between FT_0 and ST_0.

Fig. 3 shows a specific embodiment of the multiplexer circuit according to Fig. 2. For each channel the pull-down bypass circuit 50 is realized with an NMOS transistor 80, 81 and the pull-up bypass circuit is realized with a PMOS transistor 90, 91, respectively. The NMOS transistor will be used as over voltage protection and the PMOS transistor will be used as under voltage protection on channels that are not selected.

A control circuit for the bypass circuits comprises NOR gates 100, 101, the output of which is connected with the gate of the NMOS transistor 80, 81, respectively. The control circuit further comprises NAND gates 110, 111, the output of which is connected with the gate of the PMOS transistor 90, 91, respectively. One input of the NOR gate 100, 101 is connected with the input voltage U_1, U_2, respectively, and the other input of the NOR gate 100, 101 is connected with the select signal $SELECT_0$, $SELECT_1$. One input of the NAND gate 110, 111 is connected with the input voltage U_1, U_2, respectively., and the other input of the NAND gate 110, 111 is connected with the inverted select signal $\overline{SELECT_0}$, $\overline{SELECT_1}$. Therefore, the input signals of the control circuit are the input voltage U_1, U_2 and the select and the inverted select signals which control the transmission gates. If a channel is not selected (SELECT = 0) and an under voltage condition occurs ($U_1 < 0$ V) the PMOS transistor 90 will be switched on. If a channel is not selected (SELECT = 0) and an over voltage condition occurs ($U_1 > 5$ V), the NMOS transistor 80 will be switched on.

Fig. 4 shows a second specific embodiment of the multiplexer circuit according to Fig. 2. A control circuit for controlling the bypass circuit comprises a sense circuit for sensing a voltage in the input channel. The sense circuit and the bypass circuit in combination form a bypass and sense circuit consisting of a sense path and a bypass path. In the bypass and sense circuit to V_{SS} the sense path comprises a PMOS transistor 130, 131 in series with an NMOS transistor 120, 121. The source of the PMOS transistor 130, 131 is connected

to said first transmission gate FT_0, FT_1 and the source of the NMOS transistor 120, 121 is connected to ground level V_{SS}. The drain of the PMOS transistor 130, 131 is connected with the drain of the NMOS transistor 120, 121. The bypass path is formed of NMOS transistor 160, 161 the drain of which is connected with the output of said first transmission gate FT_0, FT_1 and the source of which is connected with V_{SS} . The gate of NMOS transistor 160, 161 is connected with the drains of the PMOS and NMOS transistors of the sense circuit. The driveability of NMOS transistor 120, 121 is very weak compared to the driveability of PMOS transistor 130, 131. For a channel that is switched off a voltage of $0.65V_{DD}$ is applied to gate of PMOS 130, 131. Both the sense path and the bypass path are switched off as long as the potential at node 70, 71 fulfils the condition $U70<0.65V_{DD}+|V_{THp}|$. When due to an over voltage at the input the voltage at node 70, 71 exceeds $U70>0.65V_{DD}+|V_{THp}|$ the sense path drives a small current to V_{SS}. Because of the big impedance of NMOS 120, 121 compared to the impedance of PMOS 130, 131 the gate voltage at the gate of bypass transistor NMOS 160, 161 increases very quickly so that this transistor changes very quickly to the conducting state. In this way a low impedance path to V_{SS} is installed when the voltage U70 is close to V_{DD}. The bypass and sense circuit to V_{SS} can be associated with an ideal switch that switches on as soon as U70 approximates V_{DD}.

The pull-up bypass and sense circuit consists of NMOS 140, 141 and PMOS 150, 151 as sense path and PMOS 170, 171 as bypass path. In the bypass path, the drain of PMOS transistor 170, 171 is connected with the output 70, 71 of said first transmission gate FT_0, FT_1 and the source is connected with power supply voltage level V_{CC}. In the sense path the source of the PMOS transistor 150, 151 is connected to power supply voltage level V_{CC} and the source of the NMOS transistor 140, 141 is connected to an output 70, 71 of said first transmission gate FT_0, FT_1 and the drains of the PMOS transistor 150, 151 and the NMOS transistor 140, 141 are

connected to each other. The gate of the PMOS transistor 170, 171 is connected with the drains of the PMOS and NMOS transistors of the sense path. The bypass and sense circuit works in an analogue way for undervoltage.

Measurements on real chips prove that a subthreshold current via closed FT_0 can occur also for valid input voltages $V_{SS}<U1<V_{DD}$ dependent on the voltage drop between drain and source of FT_0. If this voltage drop is significant leakage is likely to occur due to the fact that the V_{DD} level in the chip (and at the gate of FT_0) is a little bit less than the V_{DD} level applied from externally and due to the big width of FT_0, which is necessary to achieve a small impedance if the input is active ADC input channel. The proposed bypass and sense circuits keep the voltage drop on FT_0 as small as possible and thus limit the subthreshold current into the pad. The reason is that both bypass and sense circuits are switched off for potentials U70 in the range $0.35V_{DD}-V_{THn}<U70<0.65V_{DD}+|V_{THp}|$, i.e. currents via FT_0 can only flow if one of the conditions $U70>0.65V_{DD}+|V_{THp}|$ or $U70<0.35V_{DD}-V_{THn}$ is fulfilled.

A small pad input leakage current is an important quality criteria for the IO circuit of an integrated circuit.

Of course, each of the embodiments according to Figs. 1 to 4 may comprise not only two but a plurality of input channels and each channel may have the pull-up and/or pull-down circuits and the second transmission gates as described above.

An ADC circuit according to the invention comprises a multiplexer circuit according to the embodiments of Figs. 1 to 4 where the output voltage U_{OUT} of the multiplexer is the input voltage for the ADC. The accuracy of such an ADC can be as good as without over/undervoltage, i.e. the over/undervoltage has no influence to the conversion result (e.g. in case of an 8-bit ADC the accuracy is +/-2 LSB with or without over/undervoltage).

C L A I M S

1. Multiplexer circuit
comprising at least two input channels (IN_0, IN_1) and an output channel (2),
each input channel (IN_0, IN_1) comprising a first transmission gate (FT_0, FT_1) which can be switched on by a select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) for connecting the input channel (IN_0, IN_1) to the output channel (2),
at least one of the input channels (IN_0, IN_1) comprising a bypass circuit (20, 21; 50, 51; 60, 61; 80, 81; 90, 91; 160, 161; 170, 171) for preventing a current flowing through the first transmission gate (FT_0, FT_1) from reaching the other input channel,
and a second transmission gate (ST_0, ST_1), characterized in that a control circuit is provided for controlling said bypass circuit.

2. Multiplexer circuit according to claim 1, wherein said control circuit controls said bypass circuit dependent upon a voltage in the input channel (IN_0; IN_1).

3. Multiplexer circuit according to claim 1, or 2,
wherein said control circuit comprises a sense circuit (120, 130; 121, 131; 140, 150; 141, 151; 100, 110; 101, 111) to control said bypass circuit (80, 90; 81, 91; 160, 161; 170, 171) by sensing a voltage in the input channel (IN_0; IN_1).

4. Multiplexer circuit according to one of claims 1 to 3,
wherein each input channel (IN_0, IN_1) comprises a bypass circuit (20, 21; 50, 51; 60, 61; 80, 81; 90, 91; 160, 161; 170, 171) and a second transmission gate (ST_0, ST_1).

5. Multiplexer circuit according to claim 4, wherein the bypass circuit (20, 21; 50, 51; 60, 61) is switched on for an

input channel (IN_0) which is not selected and is switched off for a selected input channel (IN_1).

6. Multiplexer circuit according to one of claims 1 to 5, wherein said bypass circuit comprises a pull-down circuit (20, 21; 50, 51; 80, 81; 160, 161) reducing an input voltage for the second transmission gate (ST_0, ST_1).

7. Multiplexer circuit according to one of claims 1 to 6, wherein said bypass circuit (20, 21) is controlled by said select signal ($\overline{SELECT_0}$, $\overline{SELECT_1}$).

8. Multiplexer circuit according to one of claims 1 to 7, wherein said bypass circuit (20, 21; 50, 51) is an NMOS transistor the gate of which is controlled by said select signal ($\overline{SELECT_0}$, $\overline{SELECT_1}$), the drain of which is connected with an output of said first transmission gate (FT_0, FT_1) and the source of which is connected with ground potential (V_{SS}).

9. Multiplexer circuit according to one of claims 1 to 8, wherein said bypass circuit comprises a pull-up circuit (60, 61; 90, 91; 170, 171) increasing an input voltage for said second transmission gate (ST_0, ST_1).

10. Multiplexer circuit according to claim 9, wherein said pull-up circuit (60, 61; 90, 91; 170, 171) is a PMOS transistor the drain of which is connected with an output of said first transmission gate (FT_0, FT_1) and the source of which is connected with a power supply voltage level (V_{CC}).

11. Multiplexer circuit according to claims 1 to 10, wherein said control circuit controls said bypass circuit by means of said select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) and an input voltage (U_1, U_2) applied to said input channel (IN_0, IN_1).

12. Multiplexer circuit according to claims 8 to 11, wherein said control circuit controls said pull-up circuit (60, 61) and said pull-down circuit (50, 51) by means of said select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) and an input voltage (U_1, U_2) applied to said input channel (IN_0, IN_1).

13. Multiplexer circuit according to claim 12, wherein said control circuit comprises a NAND gate (110, 111) the output of which is connected with the gate of said PMOS transistor (90, 91) and a NOR gate (100, 101) the output of which is connected with the gate of said NMOS transistor (80, 81).

14. Multiplexer circuit according to claim 13, wherein said NAND gate receives the input voltage and the inverted select signal ($\overline{SELECT_0}$, $\overline{SELECT_1}$) and said NOR gate receives the input voltage and the select signal ($SELECT_0$, $SELECT_1$).

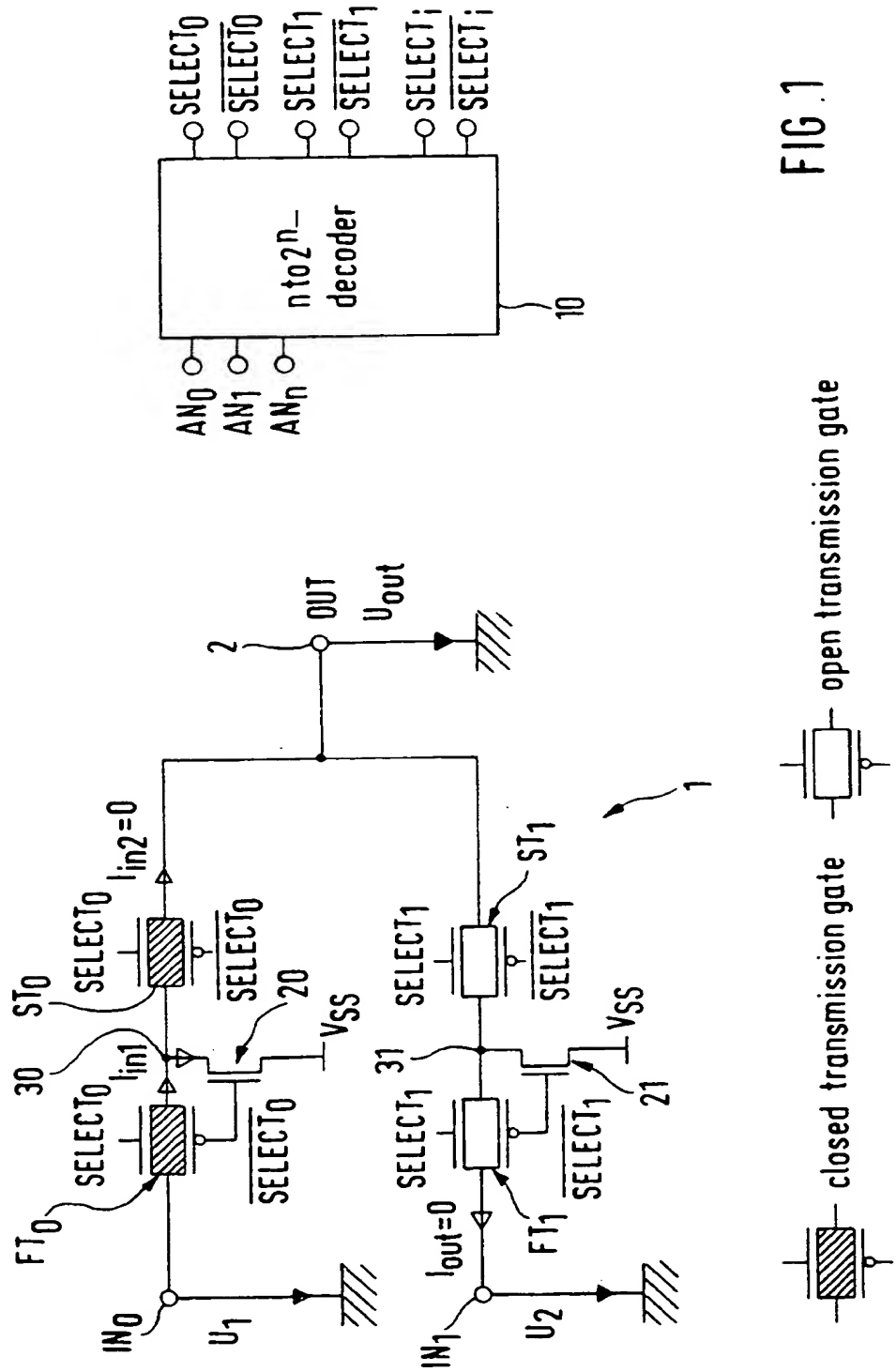
15. Multiplexer circuit according to one of claims 2 to 10, wherein said sense circuit (120, 130; 121, 131; 140, 150; 141 151) is formed so as to sense a voltage in the input channel (IN_0, IN_1) at the input of said first transmission gate (FT_0, FT_1)or between said first transmission gate (FT_0, FT_1) and said second transmission gate (ST_0, ST_1).

16. Multiplexer circuit according to claim 15, wherein a pull-down bypass circuit is formed of a NMOS transistor (160; 161) the drain of which is connected with an output (70, 71) of said first transmission gate (FT_0, FT_1) and the source of which is connected with the ground level (V_{SS}) and wherein said sense circuit is formed of a PMOS transistor (130; 131) and an NMOS transistor (120; 121) in series the source of the NMOS transistor (120; 121) being connected to ground level (V_{SS}) and the source of PMOS transistor (130; 131) being connected to an output (70, 71) of said first transmission gate (FT0, FT1) and wherein the drains of said PMOS transistor (130; 131) and said NMOS transistor (120; 121) are connected

to each other and to the gate of the NMOS bypass transistor (160; 161).

17. Multiplexer circuit according to claim 15 or 16, wherein said pull up bypass circuit is formed of a PMOS transistor (170; 171) the drain of which is connected with an output (70; 71) of said first transmission gate (FT_0, FT_1) and the source of which is connected with power supply voltage level (V_{CC}) and wherein said sense circuit is formed of a PMOS transistor (150; 151) and an NMOS transistor (140; 141) in series the source of the PMOS transistor (150; 151) being connected to power supply voltage level (V_{CC}) and the source of the NMOS transistor (140; 141) being connected to an output (70; 71) of said first transmission gate (FT_0, FT_1) and wherein the drains of the PMOS transistor (150; 151) and the NMOS transistor (140; 141) are connected to each other and to the gate of the PMOS bypass transistor (170, 171).

18. Analogue-to-digital converter comprising a multiplexer circuit according to one of claims 1 to 17.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Uout
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closed transmission gate
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SELECT0
20
Vss
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FT0
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FIG 1

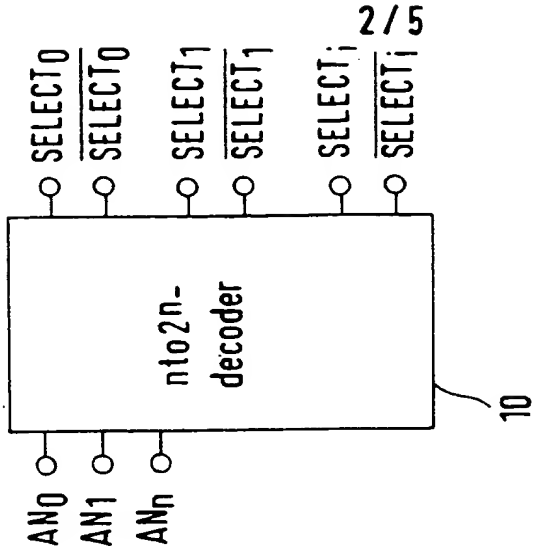
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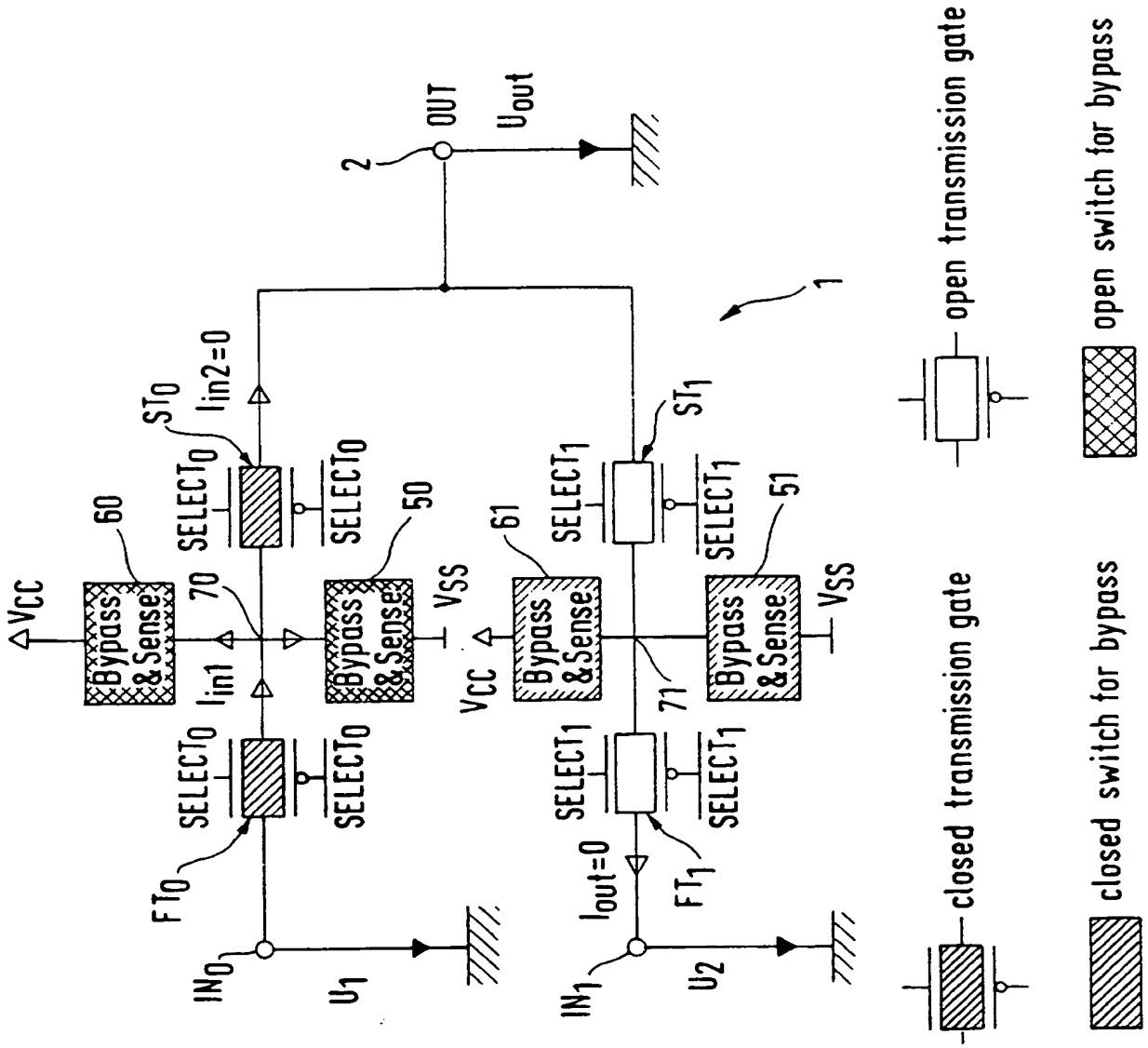
FIG.2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ST0
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SELECT0
SELECT0
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50
Vcc
Bypass & Sense
70
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U1
61
ST1
SELECT1
SELECT1
51
71
Iout=0
FT1
IN1
U2
open transmission gate
open switch for bypass
closed transmission gate
closed switch for bypass

FIG.3

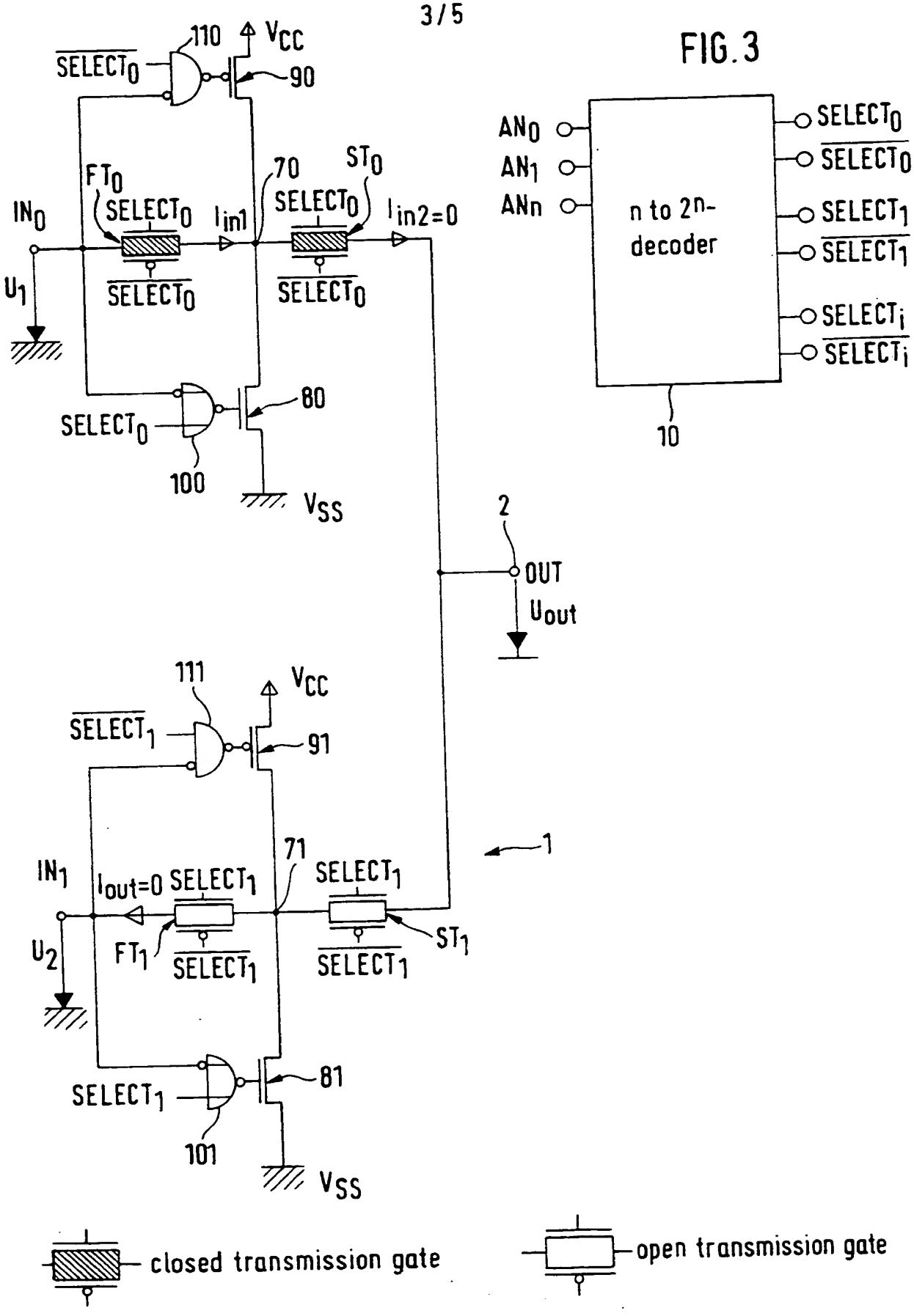
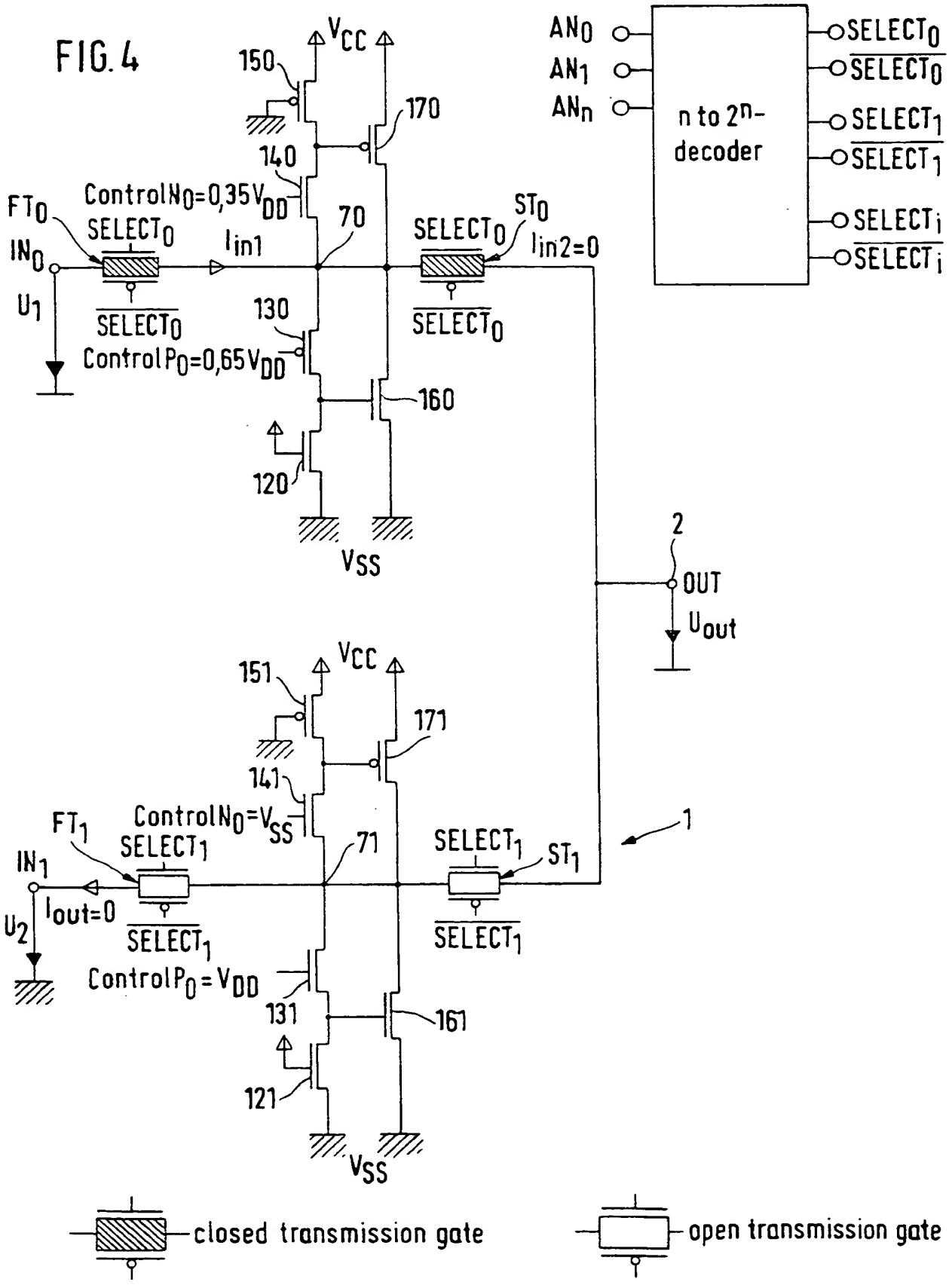

110
V_{CC}
$\overline{SELECT_0}$
90
FT_0
$SELECT_0$
I_{in1}
70
$SELECT_0$
ST_0
$I_{in2=0}$
IN_0
U_1
$\overline{SELECT_0}$
$\overline{SELECT_0}$
$SELECT_0$
80
100
V_{SS}
2
OUT
U_{out}
111
V_{CC}
$\overline{SELECT_1}$
91
71
IN_1
$I_{out=0}$
$SELECT_1$
$SELECT_1$
ST_1
U_2
FT_1
$\overline{SELECT_1}$
$\overline{SELECT_1}$
1
$SELECT_1$
81
101
V_{SS}
AN_0
AN_1
ANn
n to 2^n-decoder
$SELECT_0$
$\overline{SELECT_0}$
$SELECT_1$
$\overline{SELECT_1}$
$SELECT_i$
$\overline{SELECT_i}$
10
closed transmission gate
open transmission gate

FIG. 4


AN_0
AN_1
AN_n
n to 2^n-decoder
$SELECT_0$
$\overline{SELECT_0}$
$SELECT_1$
$\overline{SELECT_1}$
$SELECT_i$
$\overline{SELECT_i}$
V_{CC}
150
170
140
$ControlN_0=0,35V_{DD}$
FT_0
$SELECT_0$
IN_0
I_{in1}
70
ST_0
$I_{in2}=0$
U_1
$\overline{SELECT_0}$
130
$ControlP_0=0,65V_{DD}$
160
120
V_{SS}
2
OUT
U_{out}
151
171
141
$ControlN_0=V_{SS}$
FT_1
$SELECT_1$
IN_1
71
ST_1
1
$I_{out}=0$
U_2
$\overline{SELECT_1}$
$ControlP_0=V_{DD}$
131
161
121
closed transmission gate
open transmission gate

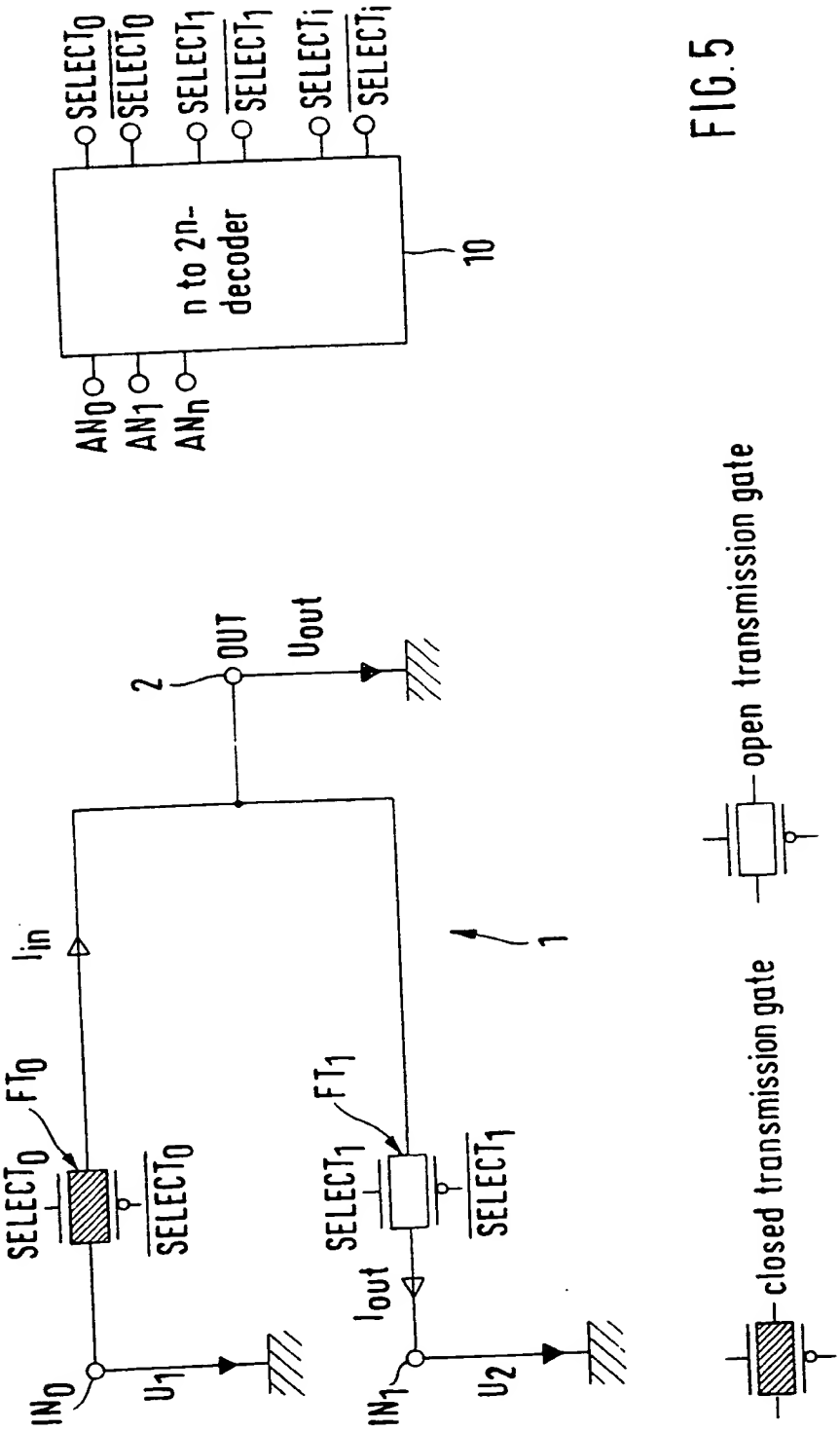

SELECT0
SELECT0
SELECT1
SELECT1
SELECTi
SELECTi
n to 2n-decoder
10
AN0
AN1
ANn
2
OUT
Uout
Iin
FT0
SELECT0
SELECT0
FT1
SELECT1
SELECT1
Iout
IN0
U1
IN1
U2
1
open transmission gate
closed transmission gate

FIG.5

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/EP 99/07531

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K17/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	GB 2 319 128 A (MOTOROLA GMBH) 13 May 1998 (1998-05-13) page 1, line 24 - line 33 page 6, line 24 -page 9, line 4; figure 6	1,2, 4-14,18
Y	SENTHINATHAN R ET AL: "APPLICATION SPECIFIC CMOS OUTPUT DRIVER CIRCUIT DESIGN TECHNIQUES TO REDUCE SIMULTANEOUS SWITCHING NOISE" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 28, no. 12, 1 December 1993 (1993-12-01), pages 1383-1388, XP000435914 page 1385, right-hand column, line 7 -page 1386, left-hand column, line 11; figure 6	1,2, 4-14,18

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 January 2000	25/01/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Cantarelli, R

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 99/07531

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2319128 A	13-05-1998	NONE	